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Flexible electronics

12-GHz Thin-Film Transistors on Transferrable Silicon Nanomembranes for High-Performance Flexible Electronics

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***M**ultigigahertz flexible electronics are attractive and have broad applications. A gate-after-source/drain fabrication process using preselectively doped single-crystal silicon nanomembranes (SiNM) is an effective approach to realizing high device speed. However, further downscaling this approach has become difficult in lithography alignment. In this full paper, a local alignment scheme in combination with more accurate SiNM transfer measures for minimizing alignment errors is reported. By realizing 1 μm channel alignment for the SiNMs on a soft plastic substrate, thin-film transistors with a record speed of 12 GHz maximum oscillation frequency are demonstrated. These results indicate the great potential of properly processed SiNMs for high-performance flexible electronics.*

1. Introduction

High-speed flexible electronics, working in the gigahertz frequency range and beyond, outperform the traditional low-speed flexible electronics in terms of power consumption and signal processing capability. In particular, high speed uniquely enables wireless capability and thus dramatically expands the applications of flexible electronics. With the high-speed, the mechanical flexibility and the dramatically reduced substrate cost, many of the current rigid-chip based electronics may be replaced by the flexible electronics for increased portability, functionality and even better performance. Such flexible electronics may be used for personal Wi-Fi devices, wearable radios, radio frequency (RF) identification devices, biomedical telemetry devices, foldable phased-array antennas, large-area radars for remote sensing, surveillance, etc.[1]

To fulfill the high speed requirement, the active semiconductor materials need to possess high mobility (and/or high saturation velocity) and to be applicable to flexible substrates, while being mechanically flexible themselves. Within these criteria, semiconductor nanomembranes (NM)[2,3] are among the best choices for high-speed flexible electronics. These materials are thin single-crystal semiconductors with very high mobilities (same as their bulk equivalents). They are transferrable to any flexible substrates and also mechanically flexible themselves.[4] In comparison to other novel high mobility materials, such as carbon nanotubes,[5,6] the planar structures and the controllable doping type of the NMs greatly ease device fabrication. Although graphene also shows the high-speed promise and may be applied to flexible substrate in the long term, currently significant challenges still remain in obtaining a sizable bandgap while simultaneously maintaining its high intrinsic carrier mobility.[7]

To transform the high mobility of the NMs into high-speed thin-film transistors (TFTs), proper processing of these materials is essential. For silicon NMs (SiNMs), effectively doping them to realize low contact resistivity and

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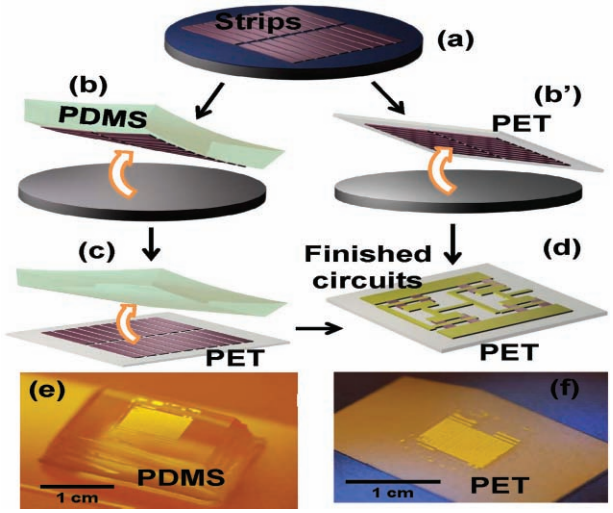

Figure 1. Illustration of SiNM transfer methods: a,b,c,d) for PDMS-assisted transfer and a,b′,d) for direct flip transfer. a) Strips are released in situ on source substrate. b) PDMS was applied to the source substrate and the strips were picked up. b′) A PET substrate coated with an adhesive layer was applied to the source substrate and lifted up the released strips. c) The strips on PDMS were print transferred to PET. d) The transferred strips were fabricated into transistors/circuits using either PDMS or direct flip transfer method. e) Strips are picked up by a PDMS stamp. f) Strips were picked up by PET substrate coated with SU-8.

low sheet resistance are critical in realizing high speed operation. Since many flexible substrates are soft and have very low processing temperature tolerance, the traditional rigid Si-chip based high-temperature processing cannot be directly applied. This challenge has been overcome by employing a predoped (via ion implantation and annealing before NM release) NM transfer and gate-after-source/drain TFT fabrication process.[8–9] These previous multi gigahertz TFTs were realized with 2.5/1.5 μm gate/channel lengths photolithography. To further improve the device speed, employing smaller feature sizes for the gate/channel at relatively low cost (other than using e-beam) is needed. However, due to the soft nature and large thermal expansion of flexible substrates, as well as NM transfer induced alignment errors, applying photolithography at smaller feature size (e.g., 1 μm and below) to the predoped SiNMs on plastic substrate has been challenging. In this paper, we report a local alignment scheme in combination with a more accurate NM transfer technique to minimize the alignment errors in each fabrication step, and thus to realize smaller feature size TFTs. It is shown that TFTs operating at over 10 GHz can be realized on large-area flexible plastic substrates.

2. Results and Discussion

As described in the previous work,[2,3] SiNMs can be created from source substrates by releasing them via undercutting the sacrificial layers or via crystal orientation-preferred wet etching.[10] These SiNMs can be either transferred with the assistance of a soft stamp[2] (as shown in **Figure 1**a,b,c,d,e) or with a direct flip transfer procedure[3] (as shown in Figure 1a,b′,d,f). Both approaches have a high transfer yield (~100%). However, the NM strip registration resolutions are different. Using the stamp-assisted transfer method, SiNMs need to be picked up by pressing the stamp toward a source substrate. Then the stamp needs to be pressed against a destination substrate coated with an adhesive layer, which is also soft until final curing. During these procedures, the NM strips will experience some position shift due to the soft nature of both the stamp and the adhesive layer. Using the direct flip transfer method, the simpler procedure causes less position shift. **Figure 2** statistically compares the registration resolutions, after curing, between these two transfer methods, where the same destination plastic substrates were coated with SU-8. A number of gaps between the transferred NM strips, as shown in Figure 2a, were measured, and the variations in the gap width in both the lateral and the vertical directions were plotted in Figure 2b,c for the polydimethylsiloxane (PDMS) assisted transfer and the direct transfer methods, respectively. Since the direct flip transfer method (as shown in Figure 2c) can realize much better (within +/–0.5 μm) registration resolution than the stamp-assisted transfer (+/–1.5–2 μm, Figure 2b), it is preferred for high-speed device fabrication. It was noted

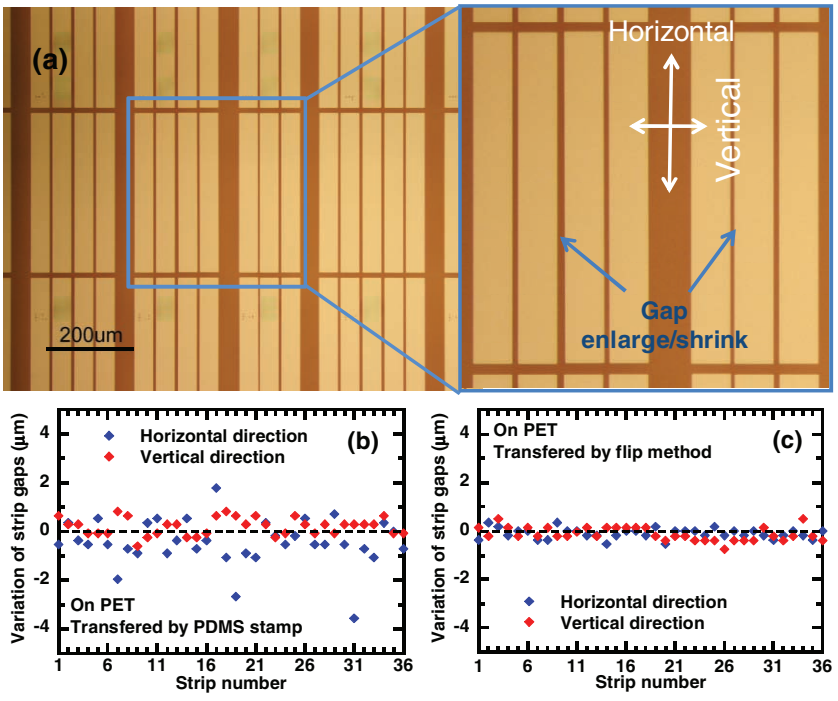

Figure 2. a) An optical microscopy image of transferred strips on a PET substrate with a zoom-in view of strip gap enlarge/shrink due to transfer. b) The statistical variations of strip gaps with PDMS stamp-assisted transfer method. c) The statistical variations of strip gaps with the direct flip transfer method.

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previously that there is a special requirement on the doping profile of the flip transferred SiNMs.[8]

Different from rigid-substrate-based device fabrication process, where 1 μm alignment can be fairly easily realized with contact-mask based photolithography, it is rather difficult to realize this alignment resolution on flexible plastic substrates such as polyethylene terephthalate (PET) due to its soft and very expandable natures. During photoresist baking (typically 115–120 °C), the PET substrates expand in size. This thermal expansion is usually anisotropic, sensitive to heating temperature, and changes with heating time. The transferred SiNM strips thus further shift their positions due to the substrate expansion. **Figure 3** shows the additional strip shift due to the PET (OC50, CPFilms Inc.) expansion after baking at 115 °C. In comparison to an unheated sample, about 0.28 μm shift per 500 μm was observed in one direction after baking for 5 min. For a chip size of 1 cm, misalignment can be as large as 5.6 μm, which is not acceptable for high-speed device fabrication. **Figure 4** shows the severity and the typical problem of the misalignment of a 0.8 cm × 0.8 cm size chip with a 2 μm critical dimension (CD), due to the SiNM strip shifts. This misalignment problem would be even worse with the devices scaled down to 1 μm and below.

In order to use the preselectively doped SiNMs[8] for high-speed devices, which can avoid high-temperature processing on plastic substrates and effectively lead to devices with high speed, an accurate alignment of the gate stack (and source/drain contacts) with these predoped SiNMs is critical. To overcome the misalignment problems, we introduce a local alignment scheme for the most critical gate photolithography steps, as illustrated in **Figure 5**. Instead of aligning the masks with the entire chip in every alignment step,[8] for the gate stack, only a small portion of the chip was aligned (by stepping) and exposed with the mask, while the rest of the chip was shielded from light. The size of the exposure area for the local alignment depends on the CD used for the fabrication and the total distortion amount caused by NM transfer and substrate baking. For a 1 μm CD, the required step size is about 2 mm according to the experimental results above. The alignment procedure was repeated until the entire chip was exposed, which is conceptually similar to using a stepper for lithography on large diameter Si wafers. The local alignment scheme increased the fabrication time (the increased

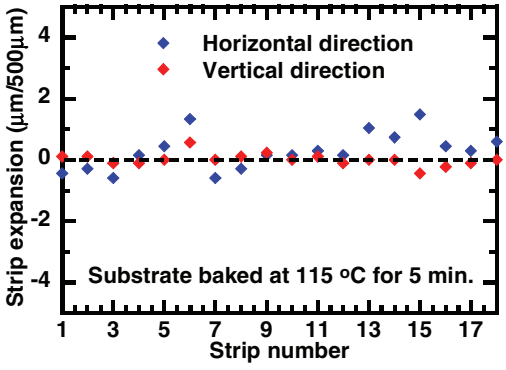

Figure 3. Strip expansion on PET substrate after baking at 115 °C for 5 min. The strip shifts are additional to those caused by transfer.

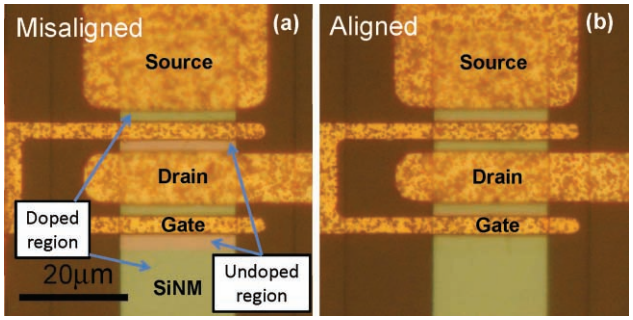

Figure 4. Microscopy images of a) misaligned and b) aligned gate stack pattern with the preselectively doped SiNM strips in the TFT lithography process. In image a, the source contact does not overlap the doped region, and the gate stack is not placed directly above the undoped channel. The misalignment is caused by both the transfer and the necessary photoresist heating procedures.

amount depends on the density of small features on a chip that require the local alignment) and thus the cost of flexible electronics. However, for high-speed (e.g., RF) flexible electronics applications, most of the area (>99%) of the flexible substrate may be covered by large passive components, that do not need the local alignment, and only a limited number of active devices require the higher precision step-and-repeat lithography for one critical mask level. As a result, the local alignment approach is a viable from the cost point of view.

With this local alignment scheme, we fabricated flexible TFTs on a PET substrate with 1 μm channel length (**Figure 6**a) for large-area flexible RF applications. The fabrication yield is almost the same across the chip in various locally aligned regions, with the exception for the very edges

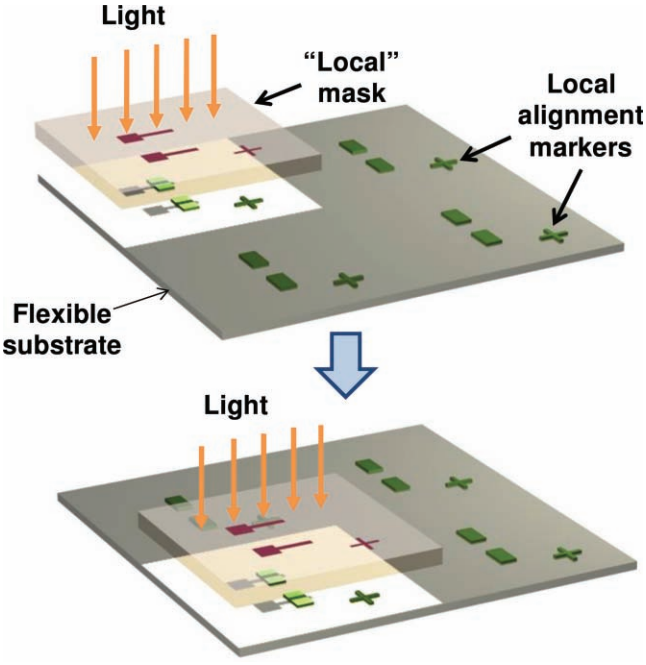

Figure 5. Schematic illustration of local alignment scheme. Devices in different regions on the flexible substrate are separately and repeatedly aligned to realize accurate alignment for the gate stack photolithography step.

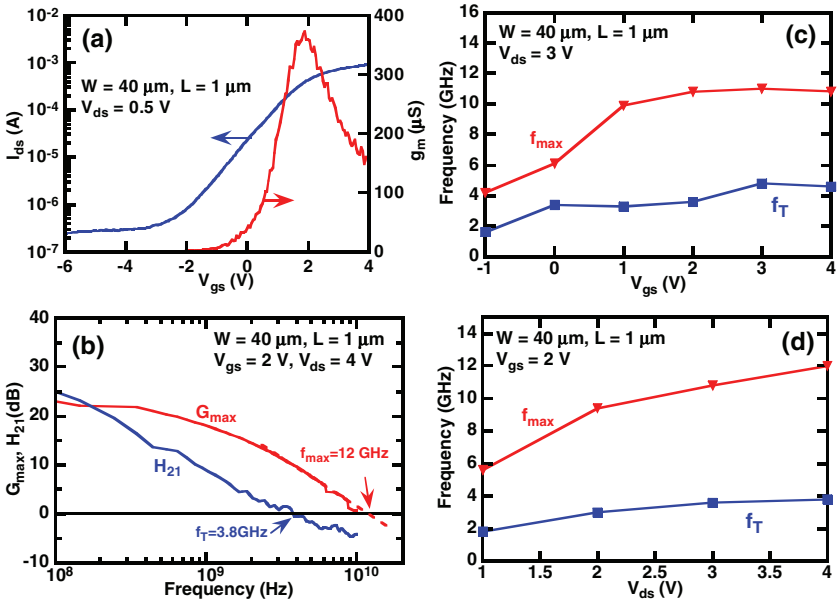

Figure 6. a) Measured transfer curve and transconductance characteristics of the 1 μm TFT. b) Measured frequency response characteristics of the TFT under V_{gs} = 2 V and V_{ds} = 4 V. c) Measured frequency dependence of the TFT on gate bias. d) Measured frequency dependence of the TFT on drain bias.

of the chip where photoresist non-uniformity caused difficulty in complete developing after exposure. Figure 6a shows the transfer curve and the transconductance of the 1 μm TFT (gate width W = 40 μm). The threshold voltage is 0.75 V and the measured maximum transduction (g_m) reaches 373 μS, which is much higher than our previous work[9] due to the smaller channel length used here. Figure 6b shows the measured cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) of the 1 μm device. Under the bias of V_{gs} = 2 V and V_{ds} = 4 V, the f_T is 3.8 GHz and f_{max} is 12 GHz. Compared with the previous work (1.5 μm channel,[9]) this 1 μm channel device exhibits about 2 times higher f_T and 1.5 times higher f_{max}. Since the rest of the device dimensions and the gate stacks are almost identical between the two devices, except for the channel length, the enhancement of f_T and f_{max} is mainly attributed to the reduction of the channel length. Figure 6c,d show the bias dependence of the f_T and f_{max}.

Figure 7 shows the bending characteristics of the device on the PET substrate with the bending direction parallel with the channel width direction (Figure 7a). The measured bending radii include 77.5, 38.5 and 28.5 mm convex, and 78 mm concave. Due to bending, the f_T exhibits slight increase and then decrease while f_{max} shows little changes with the bending. The changes of f_T are due to the changes of electron mobility under tensile strain in the device channel. The bending characteristics of the devices along the channel length direction could not be measured at the moment because the probing RF pads of the devices became inaccessible by RF probes under such a bending direction.

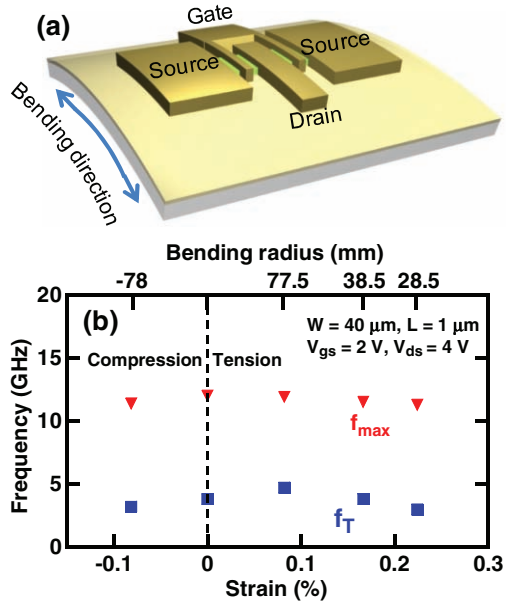

Figure 7. a) Illustration of bending test for the TFT on PET. b) Measured f_T and f_{max} variations under different bending radii.

3. Conclusion

In summary, we demonstrated that minimum device features in transferrable single-crystal SiNM can be scaled

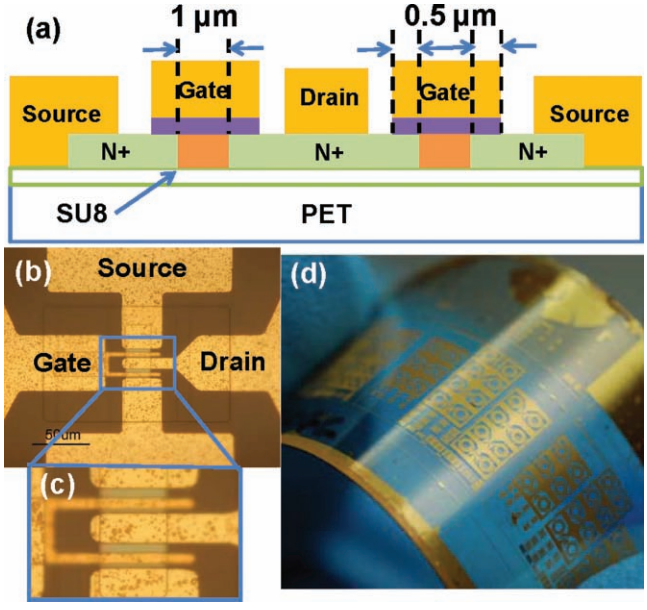

Figure 8. a) Cross-section illustration of the TFT on PET with the channel length and the overlap distances between gate and source/drain shown. b) Microscope image a two-gate-finger TFT. c) Zoom-in view of accurate gate alignment realized with the local gate alignment procedure. d) Image of a TFT array on a bent PET substrate.

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down further by improving transfer techniques and modifying lithography procedures. With a direct flip transfer method having better registration resolution and a local alignment scheme applied to the most critical gate alignment step, devices with a 1 μm channel length were made on preselectively doped SiNMs. A f_T of 3.8 GHz and a f_{max} of 12 GHz, a new record speed, were realized for flexible TFTs on soft plastic substrates. The demonstrations further indicated the great potential of the properly processed SiNMs for high-performance flexible electronics. Since the local alignment scheme is only applied to one process step, the overall fabrication TFT process is still cost effective.

4. Experimental Section

The process flow, except for the gate alignment that was performed with the local alignment method, is identical to the previously demonstrated one.[8] The process parameters for this fabrication are briefly listed here. The silicon-on-insulator source substrate has 270 nm top Si(100) layer with a buried oxide layer of 200 nm. The phosphorus energy and dose for the prerelease ion implantation are 15 keV and 1×10^{16} cm^{-2}, respectively. The spacing between the source and the drain for ion implantation is 1 μm and the gate-to-source and gate-to-drain overlap distance is 0.5 μm each (see **Figure 8**a for the device cross-section). The post-ion implantation annealing condition is 950 °C in a N_2 ambient and the annealing time is 45 min. With the local alignment method for the gate lithography, a 120 nm silicon monoxide (SiO) film is evaporated as the gate dielectric and a 30 nm Ti followed by 400 nm Au are used for the gate electrode. Figure 8b shows a two-gate-finger TFT with the zoomed-in alignment of the gate versus the doped SiNM layer shown in Figure 8c. Figure 8d shows an array of such devices on a bent PET substrate. These devices were integrated with flexible inductors and capacitors[11] on the same substrate.

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